IN THE CLAIMS

The following listing of claims replaces all previous versions, and other listings, of claims in this application.

1. (Original) A semiconductor memory device, comprising:

a plurality of memory cells;

a current sense amplifier; and

a feedback circuit to adjust a gain of the current sense amplifier depending on relative delays of data stored in different ones of the memory cells to be read on the current sense amplifier.

2. (Original) The device of claim 1, in which the feedback circuit

includes a replica of a reference one of the memory cells, and

is adapted to determine the delay of any one of the reference cells relative to an emulated delay of the reference memory cell.

3. (Original) The device of claim 2, in which

each of the memory cells is connected to the amplifier through a data IO line pair, and

the reference memory cell is the one with the shortest data IO line pair.

4. (Original) The device of claim 2, in which

the feedback circuit outputs a bias voltage determined by the determined delay, and

the current sense amplifier receives the bias voltage and adjust accordingly the gain.

5. (Original) The device of claim 4, in which the feedback circuit includes

an input impedance circuit to generate intermediate output voltages in response to the bias voltage, and

a bias amplifier to generate the bias voltage in response to the intermediate output voltages.

6. (Currently Amended) A semiconductor memory device, comprising:

~~a memory cell array including~~ a plurality of memory cells;

a plurality of data IO line pairs; ~~connected to a plurality of local data IO line pairs of the memory cell array;~~

a plurality of first current sense amplifying means ~~for controlling~~ configured to control a loop gain in response to a control signal, and ~~for~~ configured to amplify~~ing~~ and output~~ting~~ a current difference of each of the plurality of ~~the~~ data IO line pairs; and

~~a current sense amplifier input impedance detecting and loop gain control signal generating means for detecting an input impedance of the plurality of the first current sense amplifying means to generate the control signal when a read command is applied.~~

a feedback circuit configured to adjust a gain of the first current sense amplifiers depending on a relative delay of data stored in different ones of the memory cells that are to be read by the first current sense amplifiers.

7. (Currently Amended) The device of claim ~~6~~ 24, ~~in which the current sense amplifier input impedance detecting and loop gain control signal generating means includes~~ wherein the feedback circuit further comprises:

a current sense amplifier input impedance detecting ~~means for generating~~ circuit configured to generate a detecting voltage to detect the input impedance of the plurality of the first sense ~~amplifying means~~ amplifiers when the read command is applied; and

a loop gain control signal generating ~~means for receiving~~ circuit configured to receive the detecting voltage to generate the control signal to indicate whether the input impedance is negative or positive.

8. (Currently Amended) The device of claim ~~6~~ 24, ~~in which each of~~ wherein each of the plurality of ~~the~~ first current sense ~~amplifying means includes:~~ amplifiers comprises:

a first current sense amplifier ~~for amplifying~~ configured to amplify a current difference of the data IO line pair to generate an output voltage and an inverted output voltage; and

a first loop gain control ~~means~~ circuit ~~for being~~ connected between the output voltage and the inverted output voltage of the first current sense amplifier, ~~reducing~~ configured to reduce a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and ~~maintaining~~ configured to maintain a voltage between the output voltage and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

9. (Currently Amended) The device of claim 8, ~~in which~~ wherein the first loop gain control ~~means includes~~ circuit comprises a first PMOS transistor.

10. (Currently Amended) The device of claim ~~6, in which~~ 7, wherein the current sense amplifier input impedance detecting ~~means includes:~~ circuit comprises:

a bit line sense amplifier ~~for amplifying~~ configured to amplify data applied in response to the read command;

a data IO gate ~~for transferring~~ configured to transfer data of the bit line sense amplifier to the data line pair in response to the read command;

a current sense amplifier load circuit ~~for applying~~ configured to apply an electric current to the data line pair in response to the read command; and

a second sense ~~amplifying means for controlling~~ amplifier configured to control a loop gain in response to the control signal and ~~amplifying~~ configured to amplify a current difference of the data line pair to generate an output voltage and an inverted output voltage,

~~in which~~ wherein the bit line sense amplifier, the data IO gate, and the current sense amplifier load circuit are configured to have a line load capacitance of from, among the plurality of ~~the~~ memory cells, the memory cell nearest to the first current sense ~~amplifying means~~ amplifier to the plurality of ~~the~~ first current sense ~~amplifying means.~~ amplifiers.

11. (Currently Amended) The device of claim 10, ~~in which~~ wherein the second current sense ~~amplifying means includes:~~ amplifier comprises:

a second current sense amplifier ~~for amplifying~~ configured to amplify a current difference of the data line pair to generate the output voltage and the inverted output voltage;

a second loop gain control ~~means for being~~ circuit connected between the output voltage and the inverted output voltage of the second current sense amplifier, ~~reducing~~ configured to reduce a voltage difference between the output voltage and the inverted output voltage in response to the control signal when the input resistance is negative, and ~~maintaining~~ configured to maintain a voltage between the output voltage and the inverted output voltage "as is" in response to the control signal when the input impedance is positive.

12. (Currently Amended) The device of claim 11, ~~in which~~ wherein the second loop gain control means ~~includes~~ comprises a second PMOS transistor.

13. (Currently Amended) The device of claim 11, ~~in which~~ wherein the loop gain control signal generating ~~means~~ circuit receives data of the data line pair of the current sense amplifier input impedance detecting circuit as the detecting voltage, ~~and~~ lowers a level of the control signal down when the input impedance of the current sense amplifier is negative, and raises the level of the control signal ~~up~~ when the input impedance is positive.

14. (Currently Amended) The device of claim 13, ~~in which~~ wherein the loop gain control signal generating ~~means includes:~~ circuit comprises:

a bias ~~means for generating~~ circuit configured to generate a bias voltage when a power voltage is applied;

a differential amplifier ~~for being~~ that is enabled when the bias voltage is applied, and ~~amplifying~~ is configured to amplify a difference of the detecting voltage to generate the output voltage; and

an output driving circuit ~~for generating~~ configured to generate the control signal in response to the bias voltage and ~~raising~~ and configured to raise a level of the control signal ~~up~~ in response to the output voltage.

15-22. (Cancelled)

23. (Original) A data read method of a semiconductor memory device including a plurality of memory cells, the method comprising:

generating a control signal to control a loop gain of a plurality of current sense amplifiers by detecting a variation of an input impedance of the current sense amplifier when a read command is applied and data are read from the memory cell nearest to the plurality of the current sense amplifiers;

controlling the loop gain of the plurality of the current sense amplifiers in response to the control signal; and

amplifying a current different of each of a plurality of data IO line pairs by the plurality of the current sense amplifiers to generate a plurality of output signals.

24. (New) The device of claim 6, wherein the feedback circuit comprises:

a current sense amplifier input impedance circuit and a loop gain control signal detecting circuit configured to detect an input impedance of the plurality of first current sense amplifiers and to generate a control signal when a read command is applied.